ABSTRACT

A technique for forming at least part of an array of a dual bit memory core is disclosed. Spacers are utilized in the formation process to reduce the size of buried bitlines in the memory, which is suitable for use in storing data for computers and the like. The smaller (*e.g.*, narrower) bitlines facilitate increased packing densities while maintaining an effective channel length between the bitlines. The separation between the bitlines allows dual bits that are stored above the channel within a charge trapping layer to remain sufficiently separated so as to not interfere with one another. In this manner, one bit can be operated on (*e.g.*, for read, write or erase operations) without substantially or adversely affecting the other bit. Additionally, bit separation is preserved and leakage currents, cross talk, as well as other adverse effects that can result from narrow channels are mitigated, and the memory device is allowed to operate as desired.